**Area Efficient Parallel Fir Digital Filter Structures For Symmetric Convolutions Based On Fast Fir Algorithm**

**ABSTRACT**

 Based on fast FIR algorithms (FFAs), this brief proposes new parallel FIR filter architectures, which are beneficial to symmetric convolutions of odd length in terms of the hardware cost. The proposed parallel FIR architectures exploit the inherent nature of symmetric coefficients reducing half the number of multipliers in the sub filter section at the expense of increase in adders in preprocessing and post processing blocks. Exchanging multipliers with adders is advantageous because adders weigh less than multipliers in terms of silicon area, and in addition, the overhead from the increase in adders in preprocessing and post processing blocks stay fixed, not increasing along with the length of the FIR filter, whereas the number of reduced multipliers increases along with the length of the FIR filter. For example, for a three-parallel 27-tap filter, the proposed structure saves 8 multipliers at the expense of five adders, whereas for a three-parallel 81-tap filter, the proposed structure saves 26multipliers at the expense of five adders still**.**

**LANGUAGE USED:**

* Vhdl/verilog

**TOOLS REQUIRED:**

* MODELSIM – Simulation
* XILINX-ISE – Synthesis